VOLTAGE LEVEL SHIFTER IMPLEMENTED BY ESSENTIALLY PMOS TRANSISTORS

ABSTRACT OF THE DISCLOSURE

A voltage level shifter includes a front stage circuit periodically generating a first control signal and a second control signal in response to a first input clock signal and a second input clock signal complementary to the first input clock signal; a switch circuit including two PMOS transistors connected between a maximum voltage and a minimum voltage in series, wherein a third control signal is outputted from a conjunction of the two PMOS transistors, and the first and second control signals are coupled to the gate electrodes of the two PMOS transistors, respectively; and a driving circuit receiving the third control signal and outputting an output clock signal having a peak-to-peak value larger than a peak-to-peak value of the input clock signal. The voltage level shifter is implemented by essentially PMOS transistors.